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Air stable complementary polymer circuits fabricated in ambient condition by inkjet printing

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ABSTRACT

Air stable complementary polymer inverters were demonstrated by inkjet printing of both top-gate electrodes and the semiconductors in ambient conditions. The p-type and n-type polymer semiconductors were also thermally annealed in ambient conditions after printing. The good performance of circuits in ambient condition shows that the transistors are not only air-stable in term of ambient humidity and oxygen, but also inert to ion migration through dielectrics from the printed gate. The result obtained here has further confirmed the feasibility of fabrication of low-cost polymer complementary circuits in a practical environment.

The recent development of high mobility and air-stable n-type organic semiconductor materials suggests that organic thin film transistors are reaching a stage where they can be industrialized, analogous to complementary metal oxide semiconductor (CMOS) [1–4]. The complementary technology has enabled the construction of digital circuits, which operate with a high robustness, a good noise margin and low power dissipation [5–9]. To realise such organic CMOS technology, there is an urgent need for low cost, size scalable fabrication processes in practical environments. There are a few conditions to be satisfied for inexpensive fabrication of complementary organic circuits. First of all, it is crucial that both p- and n-channel semiconductors are deposited and patterned in ambient conditions. Secondly, it is desirable to avoid mask alignment processes and minimise vacuum processes for both electrode patterning and material annealing. To this end, inkjet printing is an appealing approach for micro depositing/patterning semiconductor and electrode materials [10–13]. Air-stable printed polymer CMOS inverters with thermally evaporated gates have been demonstrated very recently [1,2]. However, a related problem is that ions in the conventional printing gate materials can migrate through polymer dielectrics with the assistance of moisture in an ambient environment and gradually degrade the performance of the devices. In this paper we demonstrate some polymer complementary circuits with p- and n-channel semiconductors and gate electrode inkjet printed in ambient conditions. All the polymer materials (semiconductor, dielectrics, and gate) were annealed in air to mimic a practical manufacturing process. Through optimization of materials and fabrication process we are able to realise a match of air-stable electrical parameters for both n- and p-channel transistors in circuits, which further confirms the feasibility of the polymer CMOS manufacture in industry environment.

Source and drain electrodes of thermally deposited Au(30 nm)/Cr(10 nm) on Corning glass substrate were patterned by photolithography and lift-off processes. Both p-type [poly(3,3‴dialkylquaterthiophene) PQT-12] and n-type {poly{[*N*,*N*0-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)}}[P(NDI2OD-T2)] semiconductor polymers were dissolved into separate 1,2-dichlorobenzene solvents at 1 wt.% before being filtered through a 5.0 μm PTFE filter. Source/drain electrodes with 1 mm channel width and 20 μm channel length were chosen to demonstrate the

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circuits. The solutions were inkjet printed on covering the channels to form a 100 nm thick layer, as measured by a Veeco Dektak 150 profilometer. The p-type semiconductor was first printed and annealed under 80 and 140 °C for 20 min each, respectively. Then the n-type semiconductor was printed and annealed at 80 °C for 20 min and 110 °C for 4 h. An 800 nm thick PMMA (polymethyl methacrylate, Mw ~350 K) dielectric dissolved in butyl acetate solution was spun upon the semiconducting layer and baked at 80 °C for 30 min. To improve the surface wettability of the dielectrics, a few nanometer (~5 nm) thick PVP (polyvinylpyrrolidone, Mw ~40 K) film was spin-coated on top of the PMMA layer. Finally, gate electrodes were inkjet printed using a PEDOT:PSS solution (poly(3,4-ethylenedioxythiophene):polystyrene sulfonic acid, H.C.Starck). All the deposition steps for organic materials described above were processed in ambient conditions.

The organic thin film transistors (OTFTs) were firstly characterized in air by using an Agilent 4156 semiconductor parameter analyzer directly after the fabrications. The second round measurement was carried out under the same condition immediately after the first round, and the corresponding transfer and output characteristics of the p- and n-type transistors recorded are shown in Fig. 1a–d, respectively. Subsequently, both printed top-gate organic transistors with the transistors were stored in a glove box in dark condition and characterised again after 7 and 30 days, respectively. The transfer characteristics in the saturation region ($V_{DS} = -40$ V for p-channel and $V_{DS} = 40$ V for n-channel transistors) and the corresponding square root of the drain current as a function of the applied gate voltages are shown in Fig. 2a–d. The typical charge mobility and current on/off ratio are 0.07 cm^2/V s and 10^4 for the p-channel transistors, and 0.02 cm^2/V s and 10^5 for the n-channel transistors, respectively. The extracted saturation mobility from the slope of the square root of drain current, $\partial\sqrt{I_{DS}}/\partial V_G$, was plotted as a function of shelf-time in Fig. 2(e). It shows no degradation over time. The good stability of our PMMA-insulated devices is attributed to the perfluorinated polymer structure of the dielectrics, which provides better encapsulation against moisture permeation.

To demonstrate the general applicability of the process which we use, inverters with complementary OTFTs using PQT-12 (p-channel) and P(NDI2OD-T2) (n-channel), respectively, were fabricated by inkjet printing both semiconductors and spin-coating the dielectric layer (PMMA). Fig. 3a shows an optical image of a fabricated inverter, where both p- and n-OTFTs have the same channel width (W) and length (L) dimensions of 1 mm and 20 μm, respectively. Fig. 3b shows the dc output characteristics for various supply voltages V_{DD} = 20–40 V. The dc gain shown in Fig. 3c was obtained from dV_{Out}/dV_{In}, and the values there imply that these devices can be used to switch subsequent stages in more complicated logic circuits. Higher V_{DD} leads to an increase in the device gain, as the inverter gain is dependent on the OTFTs transconductance. For this inverter the dc gain value can be as large as −6.2 at $V_{DD} = 40$ V. The inverting voltage V_{inv} is reached when both transistors are operating in saturation and is expressed by Eq.(1)

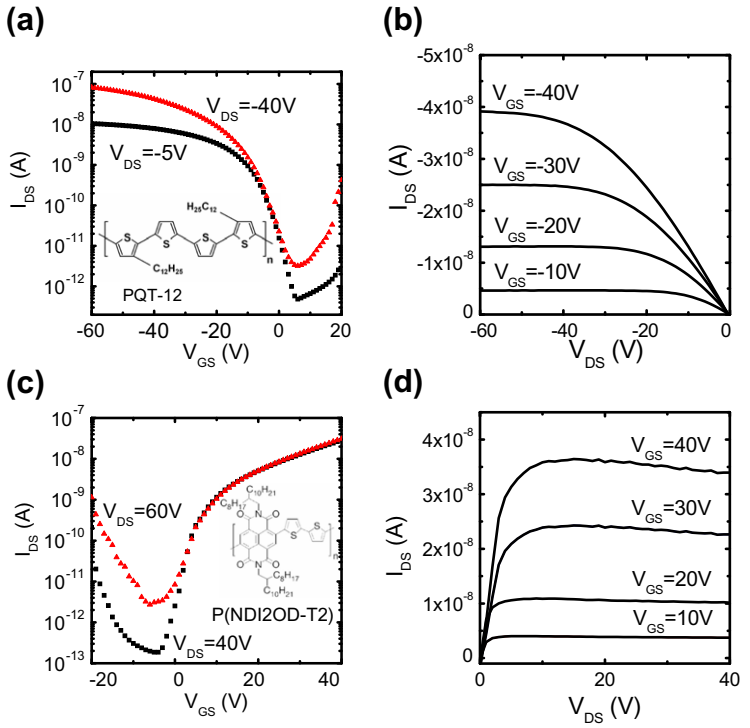

Fig. 1. Representative transfer and output characteristics of the complementary OTFTs, with (a) and (b) for p-channel transistor; (c) and (d) for n-channel transistor, respectively.

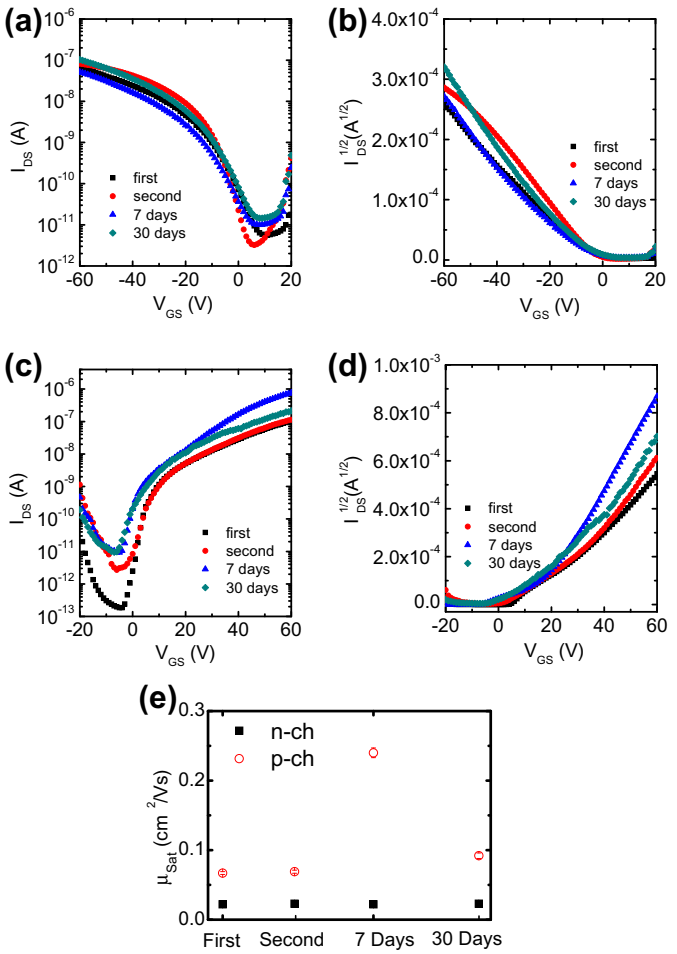

Fig. 2. (a) Transfer characteristics and (b) the square root of drain current of a typical p-channel transistor (PQT-12) measured firstly directly after the fabrications followed immediately by the second measurement, and 7 and 30 days later; (c) transfer characteristics and (d) the square root of drain current of a typical n-channel transistor [P(NDI2OD-T2)] measured in the same sequence; (e) the saturation mobility calculated from the slope of the square root of drain current for each measurement.

$$V_{inv} = \frac{V_{DD} + V_T^p + V_T^n\sqrt{\mu_n/\mu_p}}{1 + \sqrt{\mu_n/\mu_p}} \quad (1)$$

where V_T is the threshold voltage and μ_p and μ_n the mobility of the p- and n-type OTFTs, respectively. The value of V_{inv} is greater than $V_{DD}/2$ due to the mobility and threshold voltage differences between p- and n-type transistors. The inverter response was recorded by applying a square wave input between 0 and + 40 V at 2 kHz, and the corresponding output waveform is shown in Fig. 3d with a V_{DD} = + 40 V. A relatively symmetric performance in the transient time, 80 μs for the rise and 100 μs for the fall, respectively, was observed. The overshooting voltage in the output at the rising and falling edges was due to capacitive charging.

The stable performance further demonstrates the robustness of both n- and p-type devices. The stability of the semiconductive materials, in particular the n-type material, is remarkable. One may attribute this to its low LUMO (lowest unoccupied molecule orbit) value (−4.0 eV) [1], however a number of other n-type materials which have similar LUMO value do not show the same good air stability [14]. We attribute the stability of the n-type semiconductor materials to the molecular packing and crystallization as well as the film morphology, such as grain size [15,16]. In order to gain some information about the film's structure, atomic force microscope (AFM) and absorption spectrum measurements were carried out on spin-coated semiconductor films. Fig. 4 shows AFM images of the n-type P(NDI2OD-T2) film after drying at room temperature (Fig. 4a) and annealing at 110 °C for 4 h (Fig. 4b). We see that the P(NDI2OD-T2) films were crystallized after drying. The post annealing would only further improve the film quality, such as to reduce crystal defects and grain boundary mismatches. The crystalline domination in the room temperature dried n-type film, is further confirmed by absorption spectrum as shown in Fig. 5a, from which shift absorption peak before and after annealing treatment was minimal. For comparison, similar investigation was also carried out on the p-type semiconductor (PQT-12) we used. For the room temperature dried

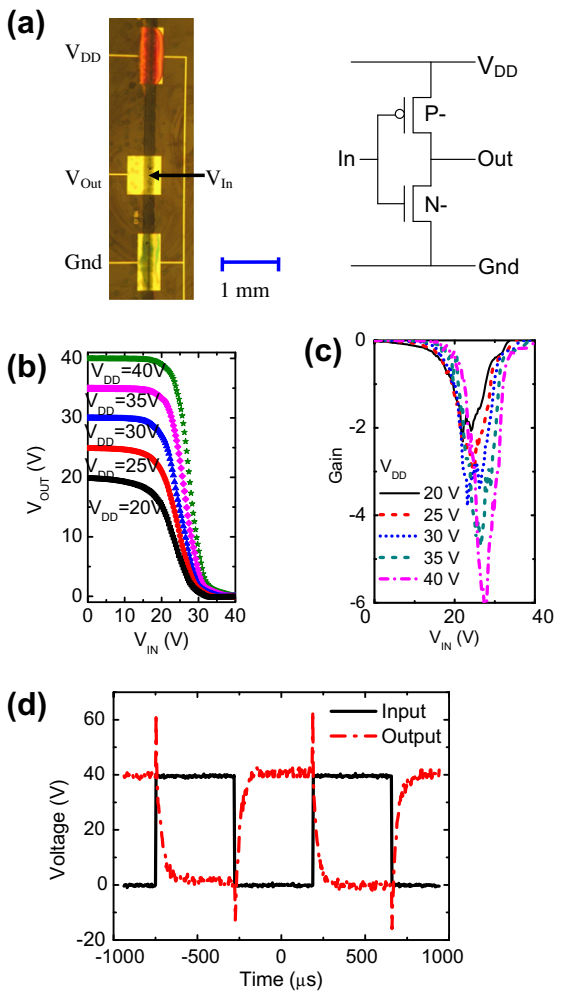

Fig. 3. PQT-12 (p-channel) and P(NDI2OD-T2) (n-channel) complementary inverters. (a) Schematic electrical connections of the inverters and optical image of the printed semiconducting devices with printed top-gate electrodes; (b) static switching characteristics; (c) dc gain; and (d) output waveform for a square wave input of 2 kHz at V_{DD} = + 40 V.

samples a crystalline structure was observed using AFM (Fig. 4c), while the existence of crystalline parts was also evidenced in absorption spectra (Fig. 5b, solid line) [17]. However, the film annealed at 140 °C showed a strong blue shift of the absorption peak and the shoulder feature disappeared (Fig. 5b, dashed line). This may be due to molecule backbone twist induced by film melting, very similar to the blue shift observed by annealing P3HT at 150 °C [18]. The AFM image of a smoother surface after the 150 °C annealing as shown in Fig. 4d was consisted with this film melting request. All AFM measurements were performed at the same scan rate of 0.271 Hz and amplitude set-point of 0.9326 V. The images were recorded with the same in-plane and height scales. The surface roughness of root mean squared value $R_q = \sqrt{\frac{1}{n}\sum_{i=1}^{n} y_i^2}$ was calculated for each obtained images, with R_q = 6.458 and 5.930 nm for n-type material dried at room temperature and 110 °C, R_q = 6.136 and 4.657 nm for p-type material dried at room temperature and 140 °C, respectively. This indicates that higher annealing temperature will smooth the finished surface of semiconductor materials and it is more effective to p-type material that n-type material.

Our inverter result shows the best matching of p-type and n-type transistors that were chosen from hundreds fabricated devices. This is because that the process condition for n-type materials is much more critical than that for p-type materials. As we know, high annealing temperature and long annealing time can usually improve the mobility of p-type materials and give a better current on/off ratio. However, our n-type material has a minimum annealing temperature of 110 °C and a maximum annealing temperature of 125 °C with a minimum annealing time of 4 h. Otherwise, it would not work. Furthermore, it was found that the current on/off ratio for the n-channel transistor reached 10^7 in the first round of characterisation as shown in Fig. 6a, but it dropped to 10^5 in the second round of measurement as shown in Fig. 6b and remained at this level unchanged in the subsequent measurements.

Threshold voltage shift (ΔV_{th}) can usually be observed in OTFTs when the gate or drain voltage is cycled. This is often due to the charge trapping in the band gap tail states [19], which is accelerated by dopant impurities such as oxygen and water [20,21] and affected by grain boundaries [22], dielectric surface modification [23], and dipolar disorder from the dielectric surface [24,25]. In addition to the charge trapping, moisture uptake and ion movement in the polymer dielectrics can also lead to ΔV_{th} [26]. Progresses have been made in controlling these factors, but it is still difficult to eliminate ΔV_{th} entirely. Fig. 6c and 6d shows the transfer characteristics of our n- and p-OTFTs measured under gate voltage cycling. The arrows there indicate the directions of the measurement. It was clear that the shift of V_{th} was small in both OTFTs.

It can be explained as the ion migration in the gate dielectrics. While a gate voltage is applied to the gate dielectrics, the ions of cation and anion migrate in opposite directions and form a space charge polarization in the gate dielectrics. Comparing the sizes of small molecule P(NDI2OD-T2) with the diameter of the free volume hole of PMMA (5.4 Å), the cations can easily migrate in the dielectric due to the molecular sieve effect of PMMA polymer chains. Also, the cations would be stabilized by the interaction with oxygen in a carbonyl group of PMMA. Therefore, the polarization of our dielectrics would be mainly due to the migration of the anions.

In summary, we successfully present the air stable complementary polymer inverters that were fabricated with printed top-gate electrodes and the semiconductors. The both p- and n-channel polymer transistors show relatively good electric performance although they were fabricated and measured in ambient condition. The stability of the n-type semiconductive material was remarkable. With AFM images, we found that P(NDI2OD-T2) films were crystallized after drying. The post annealing would only reduce crystal defects and grain boundary mismatches. It was further confirmed by absorption spectrum, in which shift absorption peak before and after annealing treatment was minimal. The similar analysis methods were used as well as in p-type semiconductive material to investigate

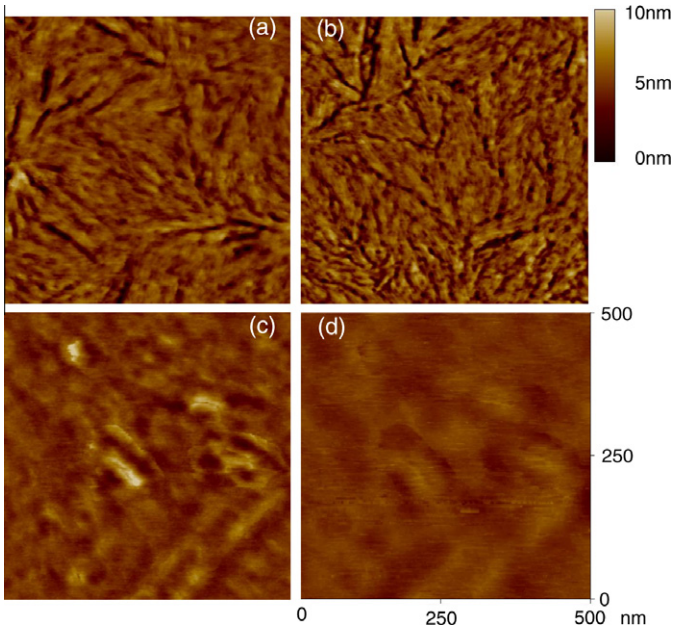

Fig. 4. Atomic force microscopy (AFM) images recorded at the same scan rate of 0.271 Hz and amplitude set-point of 0.9326 V, respectively. The images were recorded with the same in-plane and height scales. Spin-coated P(NDI2OD-T2) film (a) dried at room temperature and (b) annealed at 110 °C for 4 hours, and spin-coated PQT-12 film (c) dried at room temperature and (d) 140 °C for 20 min, respectively.

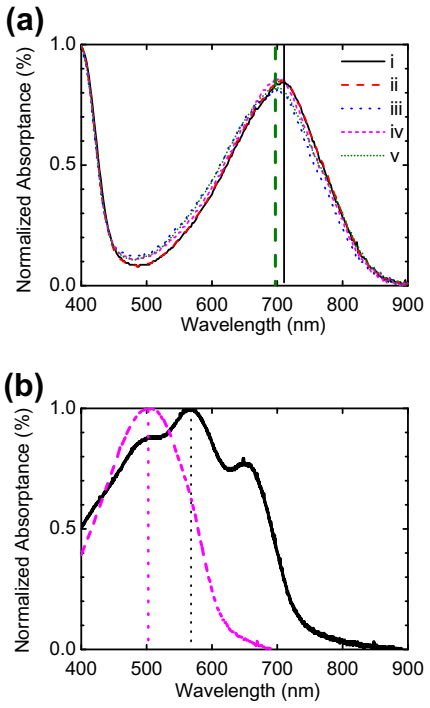

Fig. 5. Normalized absorptance of (a) spin-coated P(NDI2OD-T2) film dried at (i) room temperature and (ii) 80 °C for 30 min; after a drying process of 80 °C for 30 min, subsequently annealed at (iii) at 110 °C for 30 min, (iv) 110 °C for 4 h, and (v) 140 °C for 30 min; (b) spin-coated PQT-12 films dried at room temperature (solid line), and annealed at 140 °C for 20 min (dashed line).

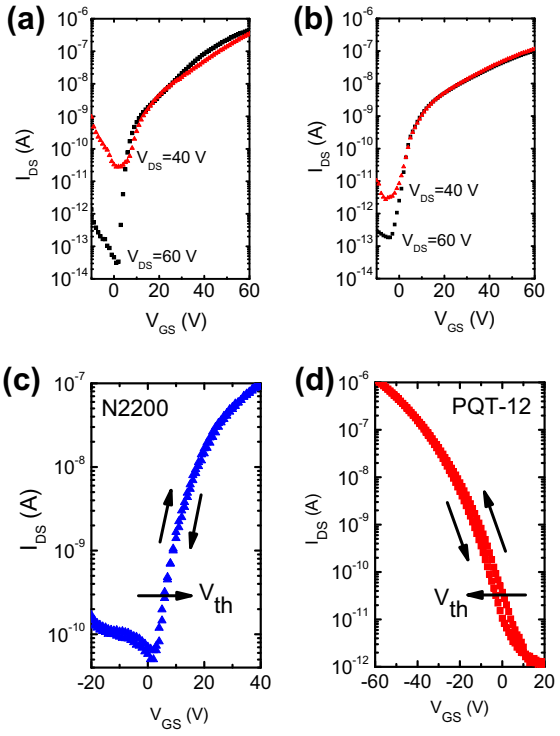

Fig. 6. Representative transfer characteristic of n-channel transistor with (a) a large on/off ratio of 10^7 at the first measurement after fabrication; (b) a small on/off ratio of 10^5 in all subsequent measurements. Gate voltage cycling effect on (c) n-type and (d) p-type OTFTs are shown, with the arrows indicate the cycling direction and shift of the threshold voltage.

the grain size. The feasibility of fabrication of low-cost polymer complementary circuits with inkjet printing tech-

nique in industrial environment has been further confirmed by our experimental results. As new generation of semiconductive, ion free printed gate materials, etc, the printed polymer CMOS can indeed be industrialized in a foreseen near future.

References

[1] H. Yan et al. Nature 457 (2009) 679.
[2] T.N. Ng et al., Appl. Phys. Lett. 94 (2009) 233307.
[3] M. Caironi et al. Appl. Phys. Lett. 96 (2010) 183303.
[4] Z. Chen, Y. Zheng, H. Yan, A. Facchetti, J. Am. Chem. Soc. 131 (2009) 8.
[5] R. Blache, J. Krumm, W. Fix, ISSCC 208 (2009).
[6] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, Nature 445 (2007) 745.
[7] D.J. Gundlach et al., J. Appl. Phys. 98 (2005) 64502.
[8] P.H. Wöbkenberg et al., Synthetic Metals 158 (2008) 468.
[9] A. Dodabalapur, Materialstoday 7 (2004) 56.
[10] H. Sirringhaus, T. Kawase, R.H. Friend, et al., Science 290 (2000) 2123.
[11] S.P. Li et al., Appl. Phys. Lett. 90 (2007) 172103.
[12] S.P. Li, D.P. Chu, C.J. Newsome, D. Russell, T. Kugler, T. Shimoda, Appl. Phys. Lett. 87 (2005) 232111.
[13] H-C. Chen et al. Journal of Display Technology 216 (2009).
[14] P.R.L. Malenfant et al., Appl. Phys. Lett. 80 (2002) 2517.
[15] H. Katz, J. Johnson, A.J. Lovinger, W.J. Li, J. Am. Chem. Soc. 131 (2009) 8.
[16] M.M. Ling et al., Adv. Mater. 19 (2007) 1123.
[17] B.S. Ong et al., Adv. Mater. 17 (2005) 1141.
[18] A. Zen et al. Adv. Funct. Mater. 14 (2004) 759.
[19] A. Salleo, R.A. Street, J. Appl. Phys. 94 (2003) 471.
[20] J.E. Northrup, M.L. Chabinyc, Phys. Rev. B. 68 (2003) 041202.
[21] M.L. Chabinyc, F. Endicott, B.D. Vogt, D.M. DeLongchamp, E.K. Lin, Y. Wu, P. Liu, B.S. Ong, Appl. Phys. Lett. 88 (2006) 113514.
[22] K. Puntambekar, J. Dong, G. Haugstad, C.D. Frisbie, Adv. Funct. Mater. 16 (2006) 879.
[23] T.N. Ng, J.A. Marohn, M.L. Chabinyc, J. Appl. Phys. 100 (2006) 084505.
[24] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, Chem. Mater. 16 (2004) 4543.
[25] T. Richards, M. Bird, H. Sirringhaus, J. Chem. Phys. 128 (2008) 234905.
[26] T.N. Ng, J.H. Daniel, S. Sambandan, A.C. Arias, M.L. Chabinyc, R.A. Street, J. Appl. Phys. 103 (2008) 044506.